## REMARKS

Claims 1-10 and 21-30 are pending in the application after the above amendments. Claim 1 has been amended, new claims 21-30 have been added, and claims 11-20 have been canceled by the present amendment. The amendments are fully supported by the specification as originally filed.

The Applicants' claimed invention is directed to a semiconductor package with a heat sink, including an interface layer having adhesion with a molding compound (for forming an encapsulant) **smaller** than adhesion between the heat sink and the molding compound. This allows the molding compound or flash left on the interface layer to be easily removable from the interface layer because of the claimed smaller adhesion, thereby making the semiconductor package free of flash.

During fabrication in a batch manner, as shown in FIGS. 2(A) to 2(H), after a heat sink module plate 23A is attached to the chips mounted on a chip carrier module plate 20A, the interface layer 233A is formed on the heat sink module plate 23A (see FIG. 2(D)); an encapsulant 24 is formed by the molding compound (see FIG. 2(E)); and a plurality of solder balls 29 are implanted on the chip carrier module plate 20A (see FIG. 2(F)). A singulation process is performed to cut through the heat sink module plate 23A, the encapsulant 24, and the chip carrier module plate 20A to form a plurality of individual semiconductor packages each having a heat sink and a corresponding chip carrier (see FIG. 2(G)). Thereafter, the singulated packages 2A are heated to remove the molding compound left on the interface layer due to the smaller adhesion and the difference in thermal expansion coefficient between the interface layer and the molding compound, such that the fabricated semiconductor packages are free of resin flash (see FIG. 2(H) and page 9, first paragraph of specification). Because the molding compound on the interface layer can be removed easily due to the claimed smaller adhesion, during a molding process for forming the encapsulant, the interface layer need not abut against an inner wall of a mold cavity, thereby avoiding the problem of cracking of the chips which can result from the clamping force produced from the mold or the heat sink module plate.

Claims 1, 2, 4-6, and 9 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 6,340,842 to Nakamura (hereinafter "Nakamura") in view of U.S. Patent 6,404,070 to Higashi et al. (hereinafter "Higashi"). Claim 3 was rejected under 35 USC 103(a) as being unpatentable over Nakamura in view of Higashi, and further in view of Morishita et al. Claims 7 and 8 were rejected under 35 USC 103(a) as being unpatentable over Nakamura in view of Higashi, and further in view of U.S. Patent 6,198,171 to Huang et al. Claim 10 was rejected under 35 USC 103(a) as being unpatentable over Nakamura in view of Higashi, and further in view of Johnson et al. Claims 11-20 also were rejected over prior art. These rejections are respectfully traversed. In view of the cancellation of claims 11-20, the Nakamura and Higashi references will be addressed in detail, with particular reference to claim 1.

The Nakamura and Higashi references, whether taken alone or in combination, fail to teach or suggest a semiconductor package or fabrication method using an interface layer having the claimed smaller adhesion with a molding compound to remove flash of the molding compound by heating, and in order to prevent cracking of the chip(s) by a clamping force.

With reference to FIG. 14, as cited in the Office Action, Nakamura discloses a Si plate 12 for accommodating a chip 22; this Si plate 12 has the same CTE (coefficient of thermal expansion) as the chip 22, thereby preventing the chip 22 from cracking by thermal stresses due to CTE mismatch (see column 4, lines 39-46). As shown in FIG. 14, the Si plate 12 provides a heat dissipation path (see arrows M and N) which allows heat from the chip 12 to pass through the Si plate 12, solder bumps 16, and electrodes 50 to the printed circuit board 14 (see column 4, lines 56-61). A metal layer 36 formed on the Si plate 12 provides another heat dissipation path (see arrows marked "L") to allow heat from the chip 22 to be dissipated into the air, to further improve the heat dissipation efficiency (see column 11, lines 57-67).

As taught in Nakamura, the metal layer 36 is provided to improve heat dissipation efficiency, but does **not** have a smaller adhesion with a molding compound to allow flash of the molding compound to be removed by heating, as recited in claim 1 of the Applicants' invention. Moreover, in Nakamura, the Si plate 12 is exposed during formation of the resin layer 28 and

thus its top surface would abut against an inner wall of a mold cavity, which could result in cracking of the chip 22 due to the clamping force of the mold or the Si plate 12, which is expressly avoided by the Applicants' claimed invention.

Higashi is directed to a semiconductor device having a heat dissipation plate, composed of a fabric of carbon fibers and a resin impregnated in the fabric, which is lighter in weight and smaller in thickness than a conventional metal plate, for mounting a chip and for ensuring good thermal dissipation and mechanical support. With reference to FIG. 1 of Higashi, as cited in the Office Action, an adhesive layer 24 is used for bonding together a circuit board 18, a heat dissipation plate 10, and a chip 12. There is no teaching or suggestion in Higashi to show that the adhesive layer 24 is an encapsulant formed by a molding process. Therefore, Higashi fails to remedy the deficiency noted in the Office Action, and thus could not be somehow combined with Nakamura to produce the Applicants' claimed invention.

Moreover, in both the Nakamura and Higashi references, there is no teaching or mounting the chip on a chip carrier such as a substrate or lead frame, as taught in the Applicants' invention. In Nakamura, the Si plate 12 serves as the chip carrier; similarly, in Higashi, the chip is mounted on the heat dissipation plate 10.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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